

Inspired by Lego

The SiLago Method: Next Generation VLSI Architectures and Design Automation

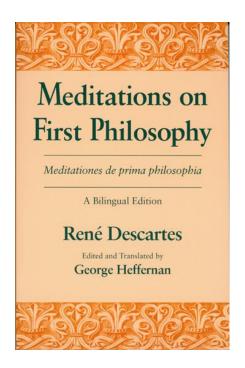
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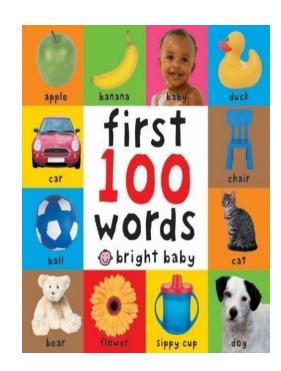
Acknowledgement:

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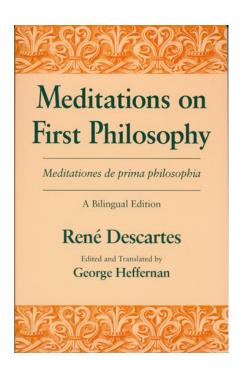




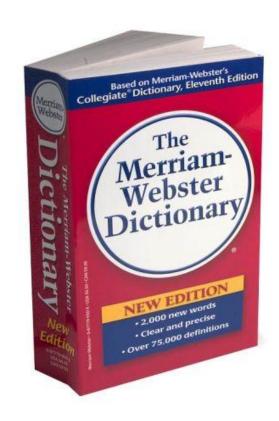
Expressed in terms of first 100 words



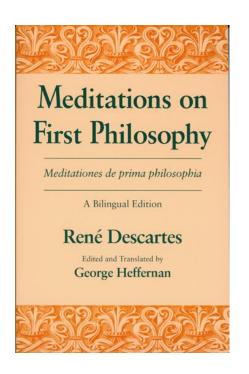




Life becomes much easier





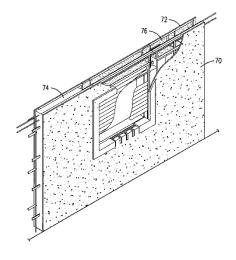


Life becomes even better



Standard Cells is too small

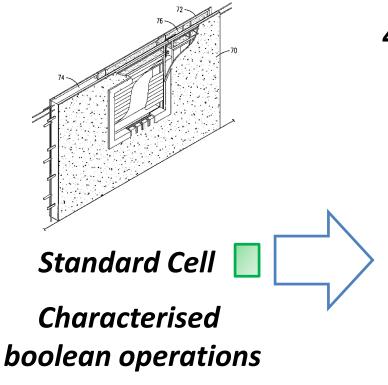






The First Proposition – Raise Abstraction to µArch level





4-5 orders larger than Sandard Cell

SiLago Blocks
Are NOT IPs – Soft or Hard

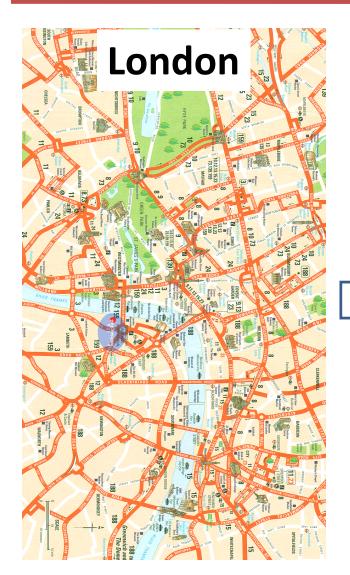
SiLago Block

(Register Files, DPUs, Switch boxes, Processors, SRAM banks etc.)

Characterised
Micro-architectural operations

Need a new Structured Physical Design Discipline





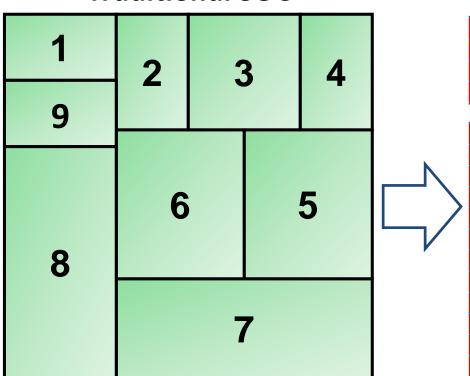




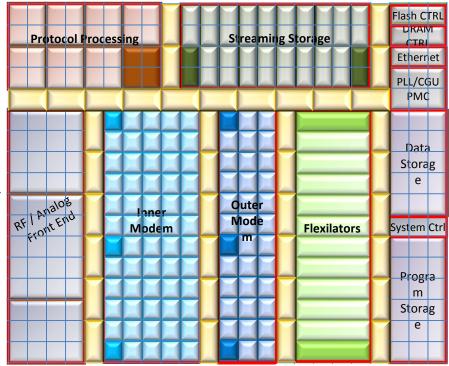
A grid based structured layout scheme



Traditional SOC

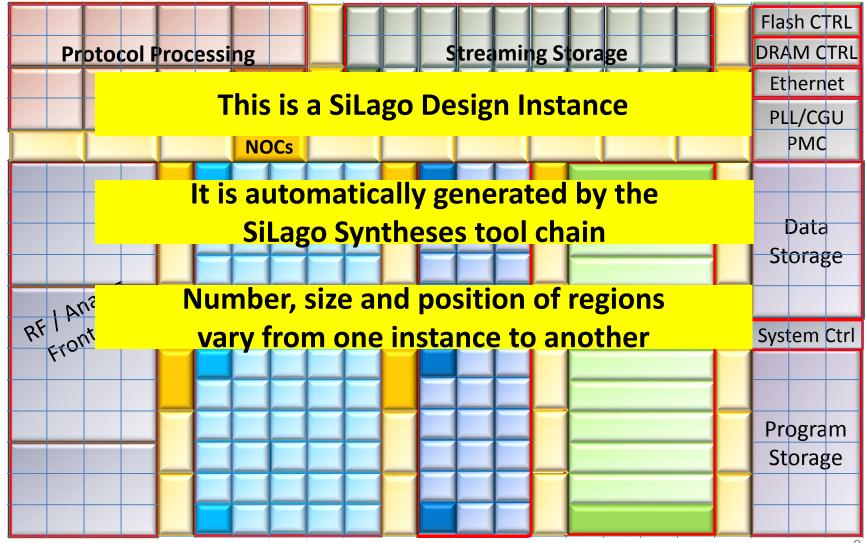


SiLago Fabric based SOC



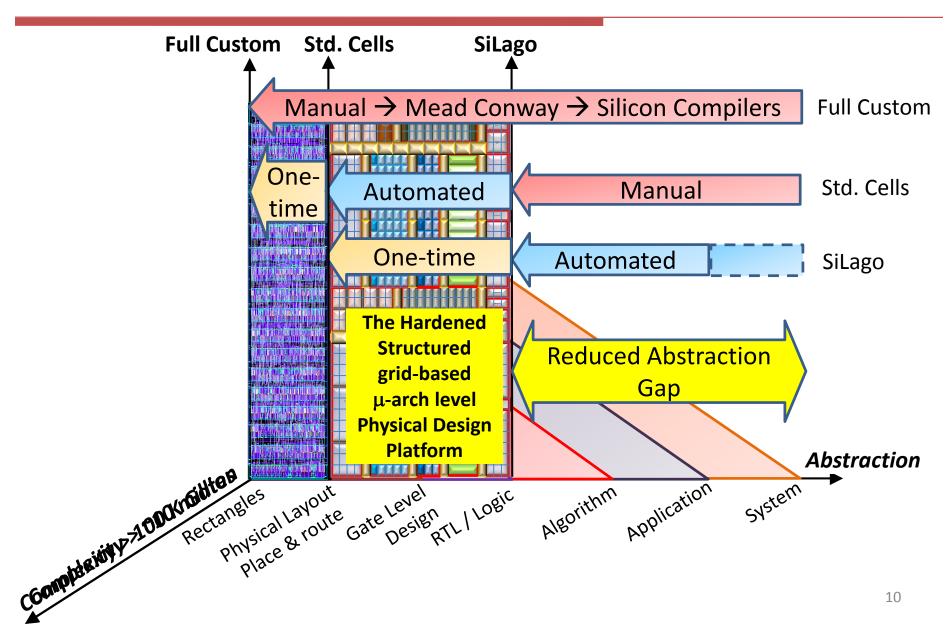
The SiLago Concepts





SiLago plotted on the VLSI Evolutionary Path

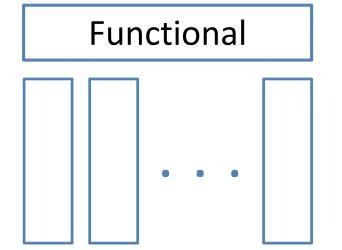




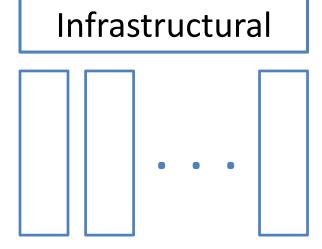
The Challenges



Higher Abstraction Vocabulary



13 Dwarfs in Berkeley Report on Landscape of Parallel Computing

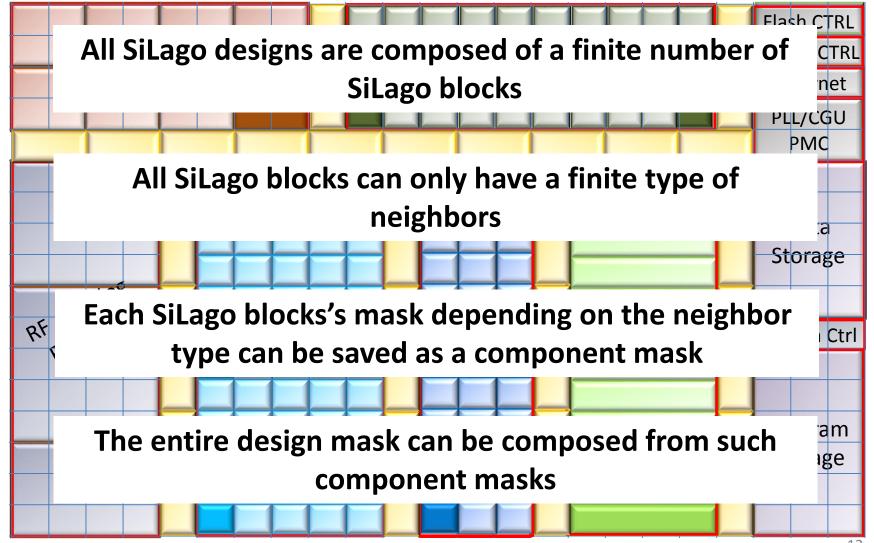


Communication, Storage, Power Management etc.

A word in the Vocabulary is not a software routine but a hardened SiLago block that composes by abutment

SiLago can reduce the mask development cost





SiLago Design Flow



